REMARKS

Applicants have amended claims 1 and 7 and added new claims 10 and 11. Claims 3 and 4 have been also amended to correct minor matters of English usage without changing claim scope.

Applicants thank the Examiner for indicating allowable subject matter.

Claims 1-6 have been rejected under 35 USC 103(a) as unpatentable over the Background of the Invention section of this application in view of U.S. Patent No. 5,081,706 (Kim). Applicants respectfully traverse this rejection.

Claim 1 states that the first FET and the second FET have gate widths of about 700 μm or less and are not connected to a shunt FET. Because of the small gate width and no shunt FET design, the claimed switching device is as small as 20% of the size of the switching devices of conventional art. See, for example, page 10, lines 9-12, of the specification.

As described at page 4, lines 10-15, of the specification, the conventional design requires that the gate width be increased to lower the insertion loss and that shunt FETs be connected to the switching FETs to compensate the reduced isolation due to the capacitance of the increased gate area. Applicants found that this conventional design guideline does not have to be followed when the signal frequency of the switching device is as high as 2.4 GHz. In particular, applicants found that at this frequency the insertion loss does not increase with reducing gate width as much as it would at the frequency of the conventional device, i.e., 1.0 GHz. This finding made the structure of claim 1, i.e., the small gate width with no shunt FETs, possible. See, for example, page 12, lines 20-27, of the specification.

The Examiner agrees that the Background section does not teach or suggest the claimed gate width. To overcome this deficiency of the Background section, the Examiner attempts to

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combine the teaching of Kim and the teaching of the Background section to arrive at the claimed invention. Applicants respectfully disagree.

Persons of ordinary skill in the art would have understood that the switching device of FIG. 6B of the Background section, on which the Examiner relies for the teaching of the claimed invention except the gate width limitation, does not operate properly at 2.4 GHz because of low isolation due to the high signal frequency. Thus, as described at page 4, lines 4-15, of the specification, persons of ordinary skill in the art would have added shunt FETs to increase the isolation that has been reduced because of the higher frequency signal, as shown in FIG. 8 of this application. In the meantime, Kim does not teach or suggest that no shunt FET is connected to the switching FETs, as claimed, by selecting an applicable signal band and gate widths most suitable for the signal band, as claimed. In fact, MESFETs 42 and 44, which the Examiner points to as teaching the claimed gate size limitation, are shunt FETs that shunt FETs connected to the Kim's switching FETs. See, for example, column 3, lines 4-10, and FIG. 5 of Kim. The Examiner also points to Kim's FIG. 2A that includes FETs with a 600 μm width gate as teaching the claimed gate width. Again, these FETs are shunt FETs as clearly understood from FIG. 2A and the related description at column 1, lines 42-51, of Kim.

Kim and the Background section of the specification together do not teach or suggest the claimed gate width size in a no shunt FET design. Thus, the rejection of claims 1-6 under 35 USC 103(a) over the Background section and Kim should be withdrawn.

Claims 7 and 9 have been rejected under 35 USC 103(a) as unpatentable over the Background of the Invention section of the specification and U.S. Patent No. 6,281,762 (Nakao). Applicants respectfully traverse this rejection.

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Claim 7 states that the first FET and the second FET have gate widths of about 700 μm or less. The Examiner admits that the Background section does not teach or suggest the claimed gate size. To overcome this deficiency, the Examiner attempts to combine the teachings of Nakao and the Background section.

Applicants point out that Nakao's switching device is a resonance-type switching device that has a switching frequency determined precisely by L and C elements of the switching device and has a capacitor (C) connecting the source and drain of Nakao's switching FET. On the other hand, the switching device of claim 7 does not include the L and C elements for resonance. Solely so that the Examiner can understand this point, and not to limit the invention, applicants have amended claim 7 to state that the signal electrodes, i.e., the gate electrode and the source electrode, of the first FET are not connected to each other and that the signal electrodes of the second FET are not connected to each other. Persons of ordinary skill in the art would not have been motivated to combine Nakao's teaching that the gate width be 600 μm and the teachings of the Background section because Nakao's gate width is meaningful only when this gate width is combined with the capacitor of 0.2 pF and the inductor of 3.9 nH, and the switching device of FIG. 6B of the Background section does not include such L and C elements. The only way persons of ordinary skill in the art would have modified the device of FIG. 6B is to connect the source and drain of the switching FET of FIG. 6B together with the gate size limitation and the added inductor, as taught by Nakao and contrary to the language of claim 7. The Examiner states that reduction in power consumption and transmission loss is the motivation to combine the teaching of the Background section and Nakao. However, this evidence is not enough to support his argument of the combination in light of the explanation above. Without more, this rejection fails. Thus, the rejection of claims 7 and 9 should be withdrawn.

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New claims 10 and 11 find support, for example, at page 5, line 23 - page 6, line 1, of the specification.

In light of the above, a Notice of Allowance is solicited.

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Respectfully submitted,

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